PRR of the PSD MPPCs and readout electronics

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Introduction (F.Guber)

The PSD (Projectile Spectator Detector) is the forward hadron calorimeter, one of important detector subsystem of the CBM experiment, which will be used for event-by-event measurements of centrality and reaction plane orientation in heavy-ion collisions. The PSD is placed between the TOF and beam dump at the distance about 10.5 m from the target, Fig.1.

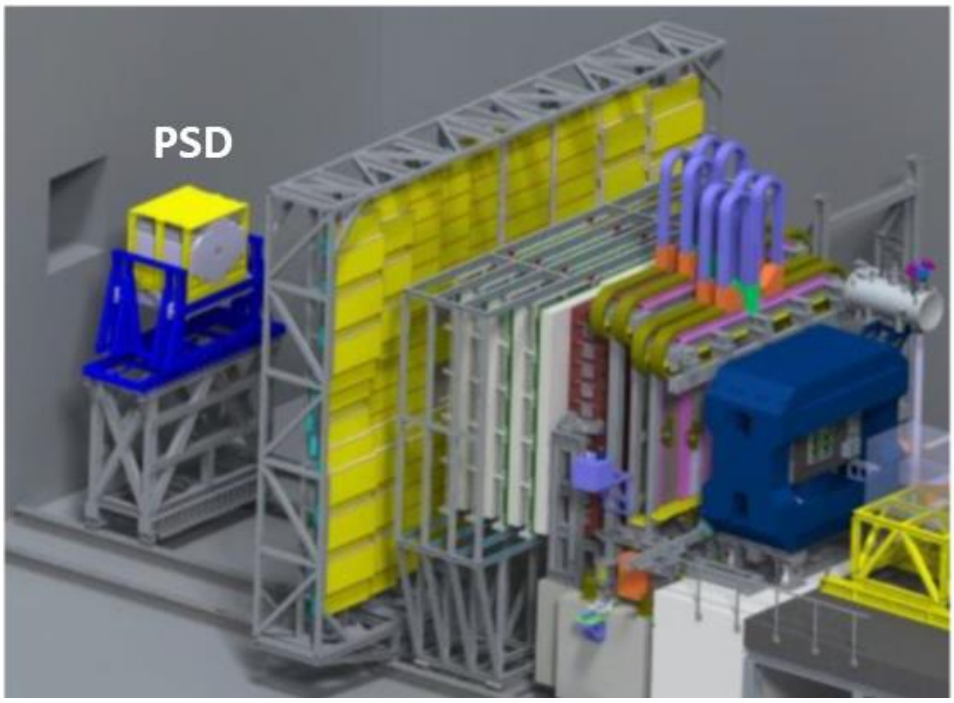


Figure 1. Schematic view of position of the PSD at the CBM.

The PSD is composed of 46 modules with transverse sizes 20 x 20 cm^2, Fig.2, left. All modules consist of 60 lead/scintillator layers with a sampling ratio 4:1 (the thickness of the lead plates and scintillator tiles are 16 mm and 4 mm, respectively). Total length corresponds to 5.6 interaction

length. All modules have longitudinal segmentations – the light is collected by WLS fibers from each six consecutive scintillator tiles on a one optic connector and detected by the single photodetector Hamamatsu MPPCs S14160- 3010P) at the end of the module, Fig.2, right. Thus, in total, 10 MPPCs are used for light detection in each CBM PSD module [1]. The light yield measured with minimum ionizing particles is about 40-50 p.e./section.

The longitudinal segmentation of modules provides the reduction of measured energy dynamic range in module and provides the uniformity of light collection along the module.

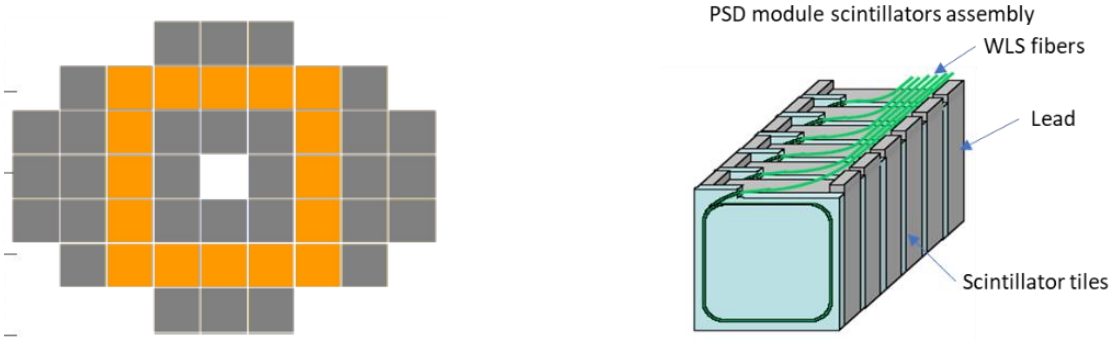


Figure 2. Schematic front view of the PSD, left, and light collection from the module, right.

All modules are already constructed and tested on cosmic muons. The PSD supermodule (array assembled from 3x3 modules) has been tested at CERN T10/T9 beamline [2]. The results shows linear PSD response in the proton energy range 1 – 9 GeV and energy resolution is in good agreement with simulated ones, Fig.3.

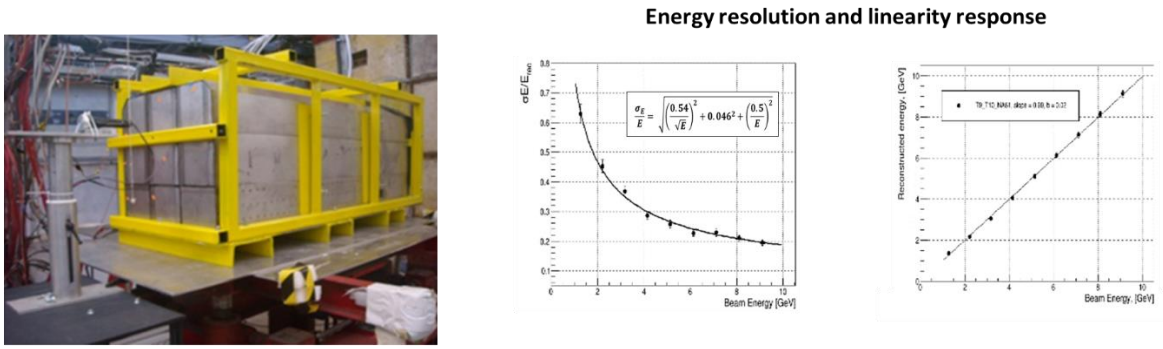


Figure 3. PSD supermodule during beam tests on T9/T10 at CERN, left. Experimental dependence of the energy resolution and linearity response of the PSD supermodule.

The PSD has the beam hole in the center. But even in this case the neutron NIEL at the end of central modules (in the plane of MPPCs in the modules) is reached the values up to 10^{11} neutrons per cm^2 during 1 month of Au beam run and interaction rate 10^6 per second. Detail study of different types of silicon photomultipliers at the high radiation conditions have been performed and the arguments for final type of MPPCs for the PSD is discussed in Section 1.

Due to high radiation conditions it was also decided to put only the boards with MPPCs, temperature sensor and LED calibration source directly in the PSD modules. All another analog and readout electronics is placed in radiation protected room which is connected with MPPCs boards with 60 m length cables. The PSD readout scheme, details of readout modules design, its characteristics have been discussed in Section 2.

Full PSD readout chain based on the ADC board for one PSD module (mPSD) has been developed, constructed and successfully tested at mCBM at high interaction rate. Details of mPSD readout and integration into mCBM DAQ based on GBT link and time synchronization are discussed. In Section 3. Here, the mPSD test results at mCBM including signal processing method with pile-up rejection or recovery are discussed.

References

[1] Guber F et al., *Technical Design Report for the CBM Projectile Spectator Detector (PSD)*,http://repository.gsi.de/record/109059/files/20150720-CBM-TDR-PSD.pdf (2015).

[2] N.Karpushkin et al., The Projectile Spectator Detector for measuring the geometry of heavy ion collisions at the CBM experiment on FAIR, NIM A, v 936, (2019) 156-157

1. MPPC Production Readiness Review (S.Morozov)

The PSD at CBM experiment will work in high radiation conditions. The schematic view of the PSD module is shown in Fig. 1 (left). The PSD module has 60 lead (16mm) + scintillator (4mm) samples which are grouped to 10 sections of six consecutive samples [1]. Thus, 10 photodetectors are mounted on the back side of each module (see Fig. 1 right). The important parameters of the silicon photo-multipliers (SiPMs) for the PSD at CBM are: high dynamic range of signals to be detected, fast recovery time of pixels to work with MHz rates and the radiation hardness. In order to select the proper sample of SiPMs existing on the market the detailed study of performance has been done for several manufacturer and variants of SiPMs.

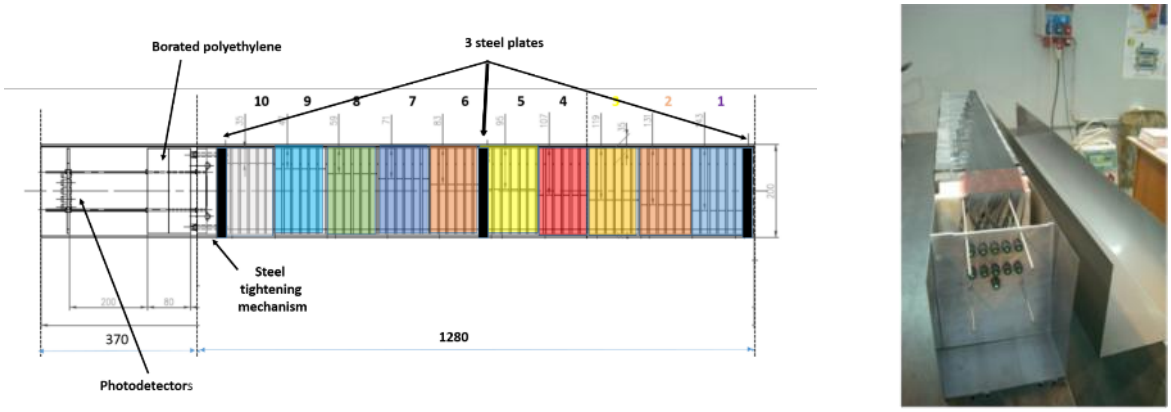


Figure 1. Schematic view of the PSD module (left) and photo of the PSD module assembling with light connectors mounted on the back side (right).

1.1 The study of irradiated SiPMs in laboratory

The study was performed for Zecotek MAPDs (3A and 3N), Hamamatsu MPPCs S12572-010P and more new S14160-3010PS, Ketek (15-WB-A0 and 50) and Sensl C30020 and B30020. All SiPMs has been irradiated with "white" spectrum of neutrons on the cyclotron of NPI (Rez, Chech Republic) with different doses from $4x10^{10}$ till $6x10^{12}$ n/cm^2 [2]. FLUKA estimated dose of radiation of photodetectors near the PSD center after one month of continuous data taking with maximum beam intensity and heaviest collision system (Au+Au) is about 10^{11} n/cm^2.

The dark current change and increasing of noise level has been measured in laboratory. All SiPMs excluding Hamamatsu show the rise of dark current from level about 1nA to 1mA (1000 times) for the dose of about $7.5x10^{11}$ n/cm^2 (see Fig.2). The Hamamatsu shows only 0.1mA in this conditions. The Zecotek 3A also shows a good performance with 0.1mA to 1mA dark current from 1 to 3 V overvoltage level. But Zecotek photodiodes have very long pixel recovery times up to 10 microseconds which is by default not fit the CBM interaction rate conditions. In the following studies the Zecotek MAPDs are used just for comparisons. The main point of interest was focused on detailed study of Hamamatsu MPPCs. The second test in LAB was the LED flash light collections and signal-to-noise ratio (SNR) estimation. The studies were done for doses from $5x10^{10}$ till $6.4x10^{12}$ and it was shown that only for the dose level of about $2x10^{12}$ (20 times of expected dose) the signal level has a very fast drop. The signal can be partially restored with HV adjustment. The SNR is measured to be changed about 10 times of expected dose of 10^{11}.

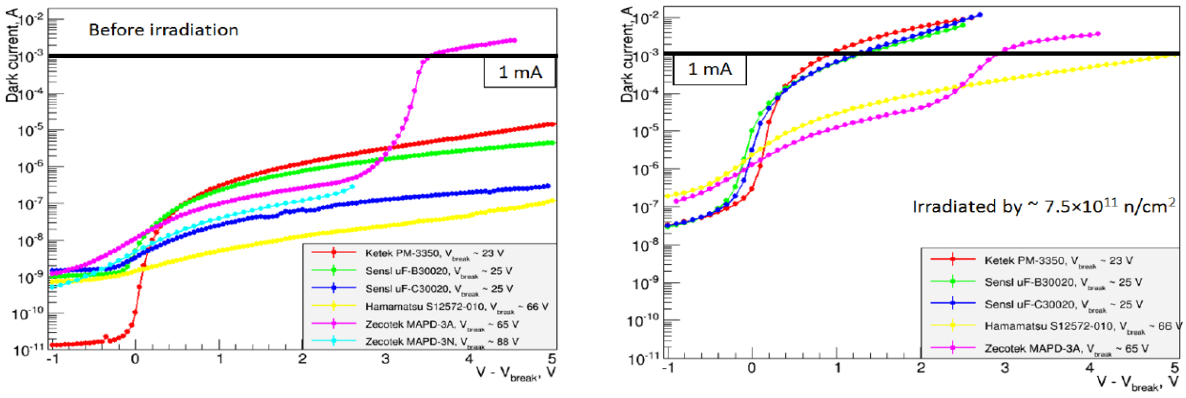


Figure 2. Results of dark current measurements for the photodiodes in laboratory.

1.2 The study of PSD performance with irradiated SiPMs on beam (CERN PS and SPS).

The PSD at the CBM is composed of 46 modules with transverse sizes 20 x 20 cm^2. The same calorimeter modules are used at the NA61/SHINE experiment on forward hadron calorimeter PSD [3]. The irradiated photodetectors were mounted on the FEE boards of one of PSD module and were tested on the PS and SPS beams at CERN. It was shown photodiodes irradiated up to the $2.5x10^{11}$ dose are still sensitive to the minimum ionization particle (MIP) signals for Hamamatsu MPPCs. The studies of calorimeter module response for the different energies of protons shows the energy resolution of about 70%/sqrt(E) which is comparable with non-irradiated photodetectors. The main drop of energy resolution is due to noise increasing level. The addition noise cut on sections will help to improve the energy resolution of calorimeter. The result of full scale energy range energy resolution for non-irradiated Hamamatsu MPPCs and irradiated with dose of about $2.5x10^{11}$ is shown in Fig. 3.

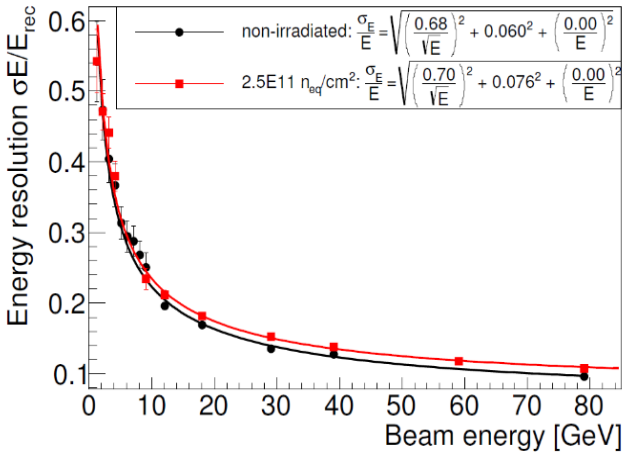


Figure 3. Energy resolution measurements for Hamamatsu MPPCs equipped module of PSD.

The drop of energy resolution has been studied for different doses of radiation (see Fig. 4 left) showing that up to 2-3 "typical" doses the drop is only about several percents. The linearity of response seems not to be changed (shown in Fig. 4 right).

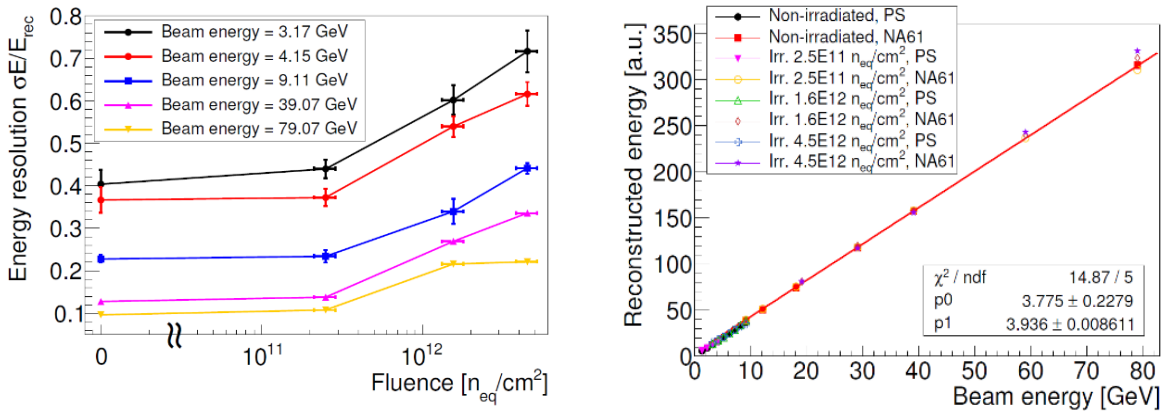


Figure 4. Energy resolution w.r.t. the irradiation dose (left) and linearity of the PSD module response for different beam energies (right) for Hamamatsu MPPCs equipped module of the PSD.

Finally, the studies show that Hamamatsu MPPC S14160-3010PS is the best choice for the performance of the PSD at the CBM at high expected interaction rate and radiation conditions.

References:

[1] Guber F et al., *Technical Design Report for the CBM Projectile Spectator Detector (PSD)*, http://repository.gsi.de/record/109059/files/20150720-CBM-TDR-PSD.pdf (2015).

[2] V. Mikhaylov et al., R*adiation hardness of Silicon Photomultipliers for CBM@FAIR, NA61@CERN and BM@N experiments*, Nucl. Instrum. Meth. A 912 (2018) 241.

[3] Golubeva M., et al., J. Phys. Conf. Ser., 798 (2017), p. 012073, doi:10.1088/1742-6596/798/1/012073

2. The PSD readout electronics Production Readiness Review

2.1 Full PSD readout chain electronics design (A.Makhnev)

Architecture of the PSD readout electronics

PSD's modules are exposed to a significant dose of ionizing radiation during operation, which limits the usage of the electronics components, mounted in the nearest proximity of the detector. Moreover, the wide dynamic range of the signals from the detector limits the usage of additional amplifiers after the MPCC.

These factors suggest splitting the detector electronics into radiation-hard part and radiation-sensitive readout part. Wide dynamic range will be achieved by omitting any kind of amplifiers between the sensors and the transmission lines. Two parts of the readout chain are to be connected with long (60m) signal cables. These include detector signal cables, HV bias cables, temperature sensors lines and calibration LED cables.

Detector electronics also includes a number of service devices: an HV bias source and a pulse generator with precise timing for generating the signals for optical calibration subsystem.

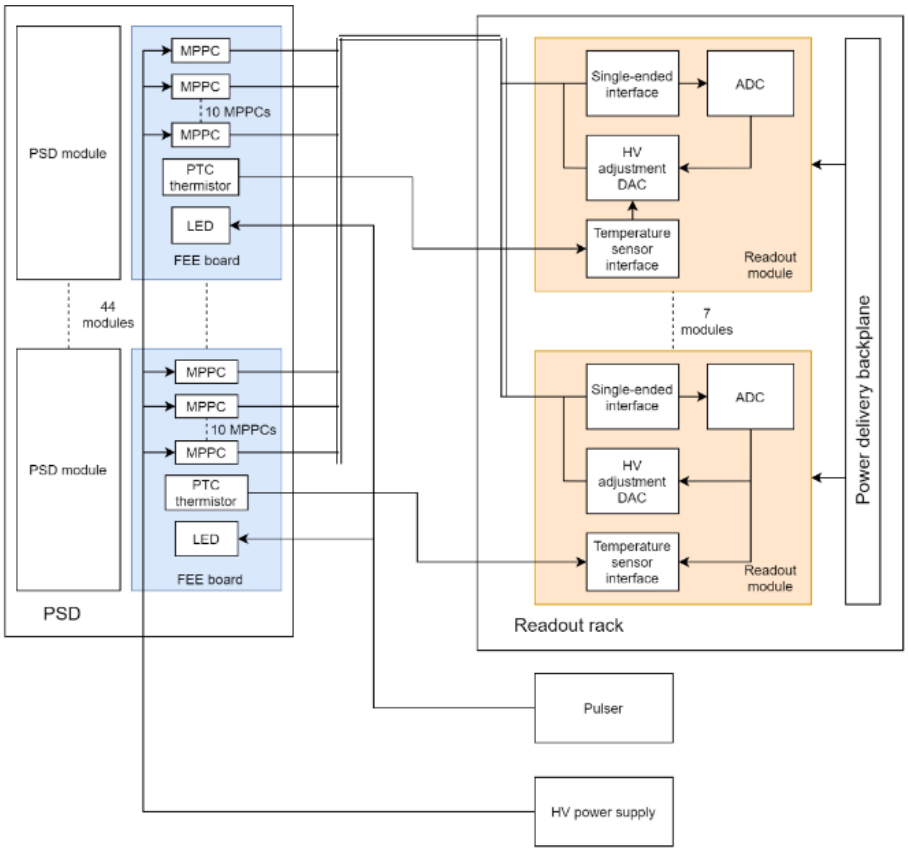


Figure 1 - PSD electronics architecture

Sensor electronics

Sensor board's (shown on Figure 2) main function is to convert optical signals from the detector modules into electrical pulses.

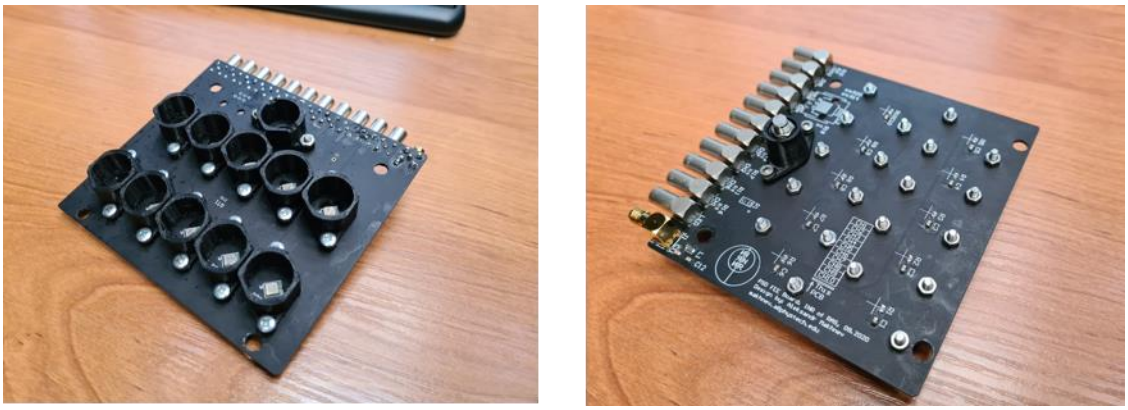


Figure 2 - Sensor board

These boards host MPPCs and a minimal number of radiation-hard components: HV bias filters,

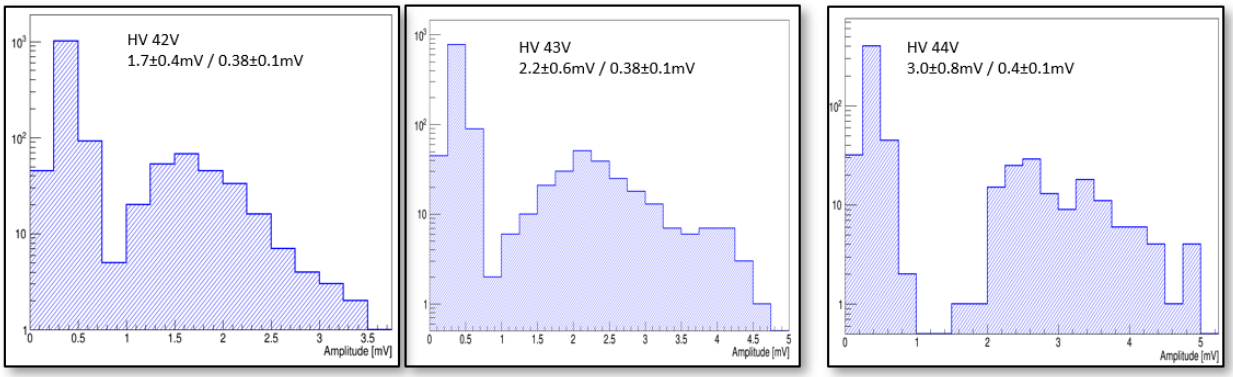


Figure 3 - Signal and pedestal separation

a temperature sensor and necessary connectors. For these boards, custom 3D-printed light protection fixtures have been developed. These include cylindrical shields around the MPPC optical coupling, that cover MPPCs from ambient light and minimize optical crosstalk and a fixture for mounting a calibration LED. Performance of these structures has been tested and showed major reduction of the dark current, from 1 uA to 80 nA per MPPC under the same ambient light conditions. These board provide sufficient signal to noise ratio and show clear separation of 1 MIP signal from the pedestal, as shown on Figure 3.

As PSD modules produce a wide range of optical signals, an MPPC with high dynamic range is needed. We have conducted several tests, in which MPPCs were illuminated with a laser light of varying intensity and linearity of the MPPCs were checked. The chosen MPPCs show good linearity over the range of 500 MIPs, as shown on figure 4.

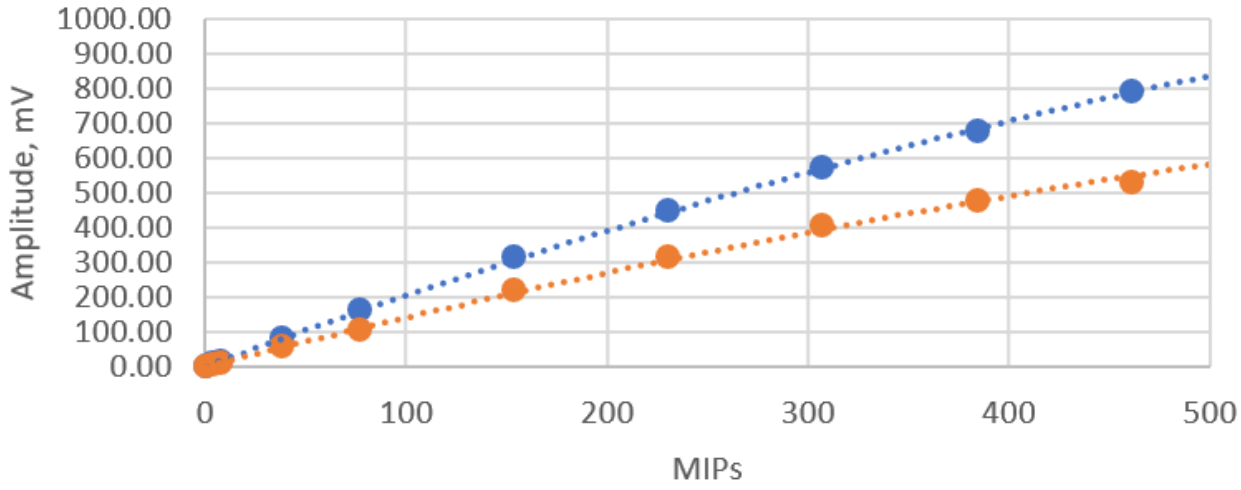


Figure 4 - MPPC signal amplitude vs optical signal intensity, blue - 1.5m cable, orange - 60m cable

Readout module

Readout module's functions include conversion and digitization of pulses from FEE boards, per-channel high voltage adjustment and providing digital interface for the temperature sensors.

Readout modules host 64 single-ended to differential converters based on AD8138 ICs. Conversion is required to interface with PANDA ADC64 board [1], which has differential inputs. These converters are built with adjustable input and output zero level settings and have an overall gain of 2 and an input voltage range of 4V. Readout modules also host a circuit for HV bias adjustment. A common uniform bias voltage is provided to all of the FEE boards. Signal lines don't have termination resistors or decoupling capacitors on the detector side, MPPCs are directly connected to the output. Each input circuit has 16-bit DAC (DAC8554 IC), which sets offset voltage on the input (from 0 to 5V), which compensates the common bias voltage provided to MPPCs. DACs are controlled by an onboard MCU, which communicates with ADC64 board via an I2C line. This setup allows per-channel adjustment of the HV bias, which is necessary for temperature compensation and gain calibration.

Latest revision of the readout module also hosts a temperature sensor interface, which is connected to the on board MCU and may be accessed by the ADC64 board.

In total, 3 revisions of Readout module have been developed, 2 of which were verified during test runs of mCBM experiment. All the circuits, related to the readout chain are tested. Common view of the readout module is shown of the Figure 5.

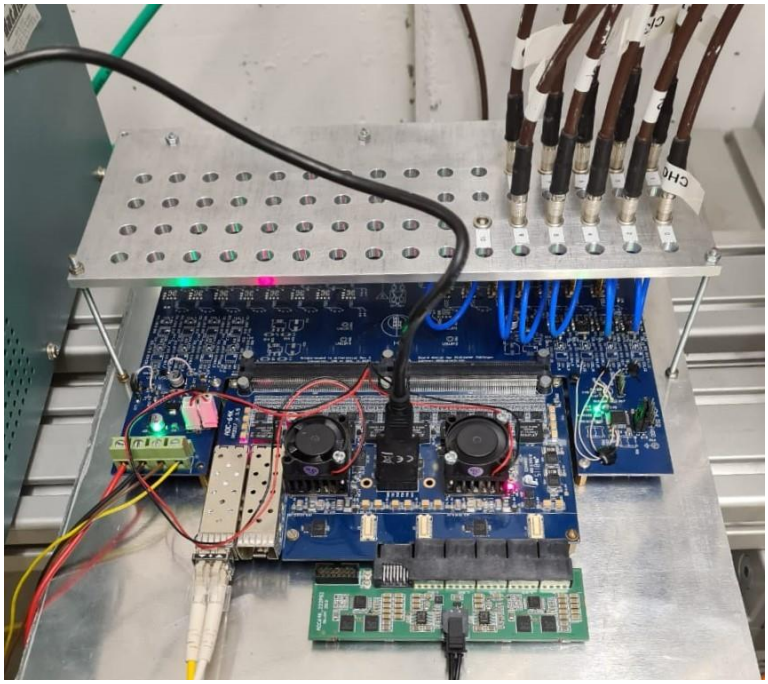


Figure 5 - Readout module

LED pulse generator

A short pulse generator is required to produce signals for calibration LEDs. Signals should have precise timing characteristics with local or remote synchronization. Current version of the generator is based on a flip-flop, which is timed by the capacitor, charged by a current source. This circuit has been tested on the pre-production PCB and operates as expected. Timing is controlled through the DAC, with ability to choose from external and internal start synchronization. Generator also includes a set of 50 Ohms output buffers, capable of driving the detector LED through a long coaxial cable. Generator is capable of providing 2-50 ns pulses with 3.3V amplitude.

HV bias source

HV bias generator consists of a DC-DC boost converter with DAC-adjustable voltage setting, capable of providing 500mA at 55V. Voltage from the converter is precisely adjusted and filtered by a linear regulator and then distributed over a set of the current monitoring circuits, one for each FEE board. These circuits include a shunt and a corresponding amplifier for current monitoring and comparators for detecting high current and overcurrent. In case of an overcurrent, bias supply is disconnected by a solid-state switch. Current monitoring circuits include necessary interfaces

for current monitoring by the ADC, which is embedded into an MCU, as well as a digital interface that provides alerts on overcurrent events. This system has been tested on a pre-production PCB and operates as expected.

Cabling

As the detector has no amplifiers after MPPCs and requires transmission of the unamplified signals over long distances, the accurate selection of the cable type is very important. To verify the proposed cabling solutions (DRAKA CB50 and РК50-3-310нг(С)-HF) we have conducted several signal integrity tests. Measured cable frequency response and a digitized signal waveform are shown on the Figure 6.

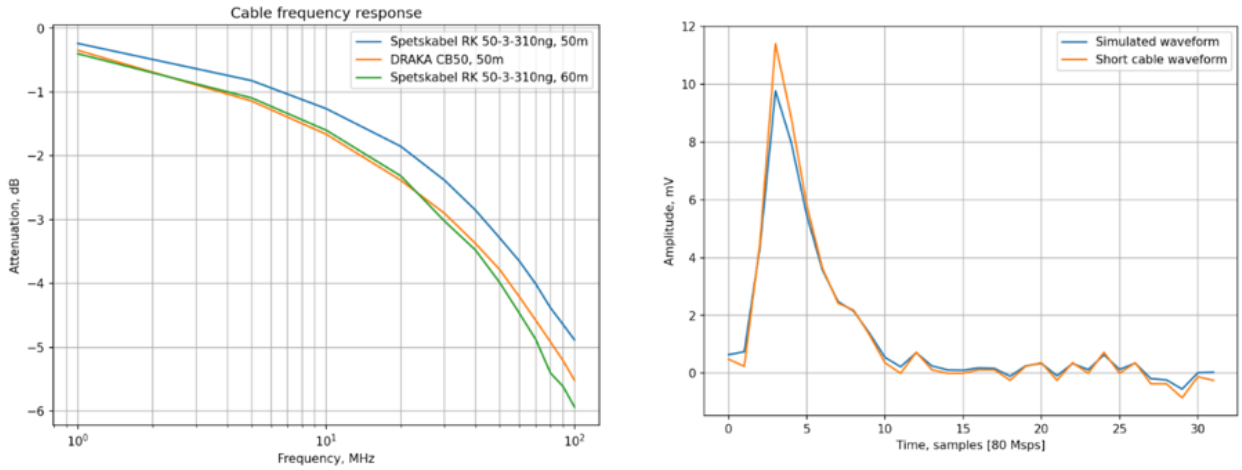


Figure 6 - Cable frequency response (left), expected signal attenuation (right)

The signal attenuation in the cabling, simulated for the input signals is around 20%. To verify this expectation, we have conducted a test, in which an MPPC was illuminated with a laser diode to produce repeatable signals, and the amplitude of the resulting pulses was measured through 1.5m and 60m cables. Waveforms, achieved in this these tests show 30% attenuation of the signal, which meets the expectation with additional attenuation, that may be explained by addition of connector losses. (Figure 7) In the latest mCBM test runs, our readout chain has been assembled with 60m cables between the detector and the readout module, and shows predicted signal attenuation and noise level.

Control circuit

Control of PSD's electronics is done by MCUs, mounted in the Readout Modules, Pulse generator and HV source. MCUs receive commands and sends data to their corresponding ADC64 board via an I2C interface. I2C interfaces of the ADC64 boards are controlled trough a GBT link. Schematic view of the control circuit is shown on the Figure 8.

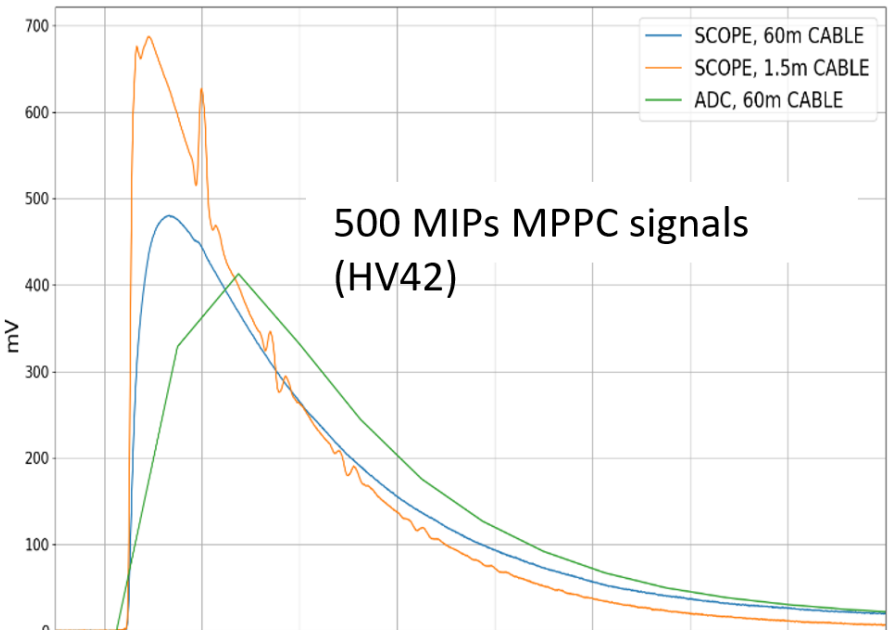


Figure 8 - Signal attenuation with actual cabling

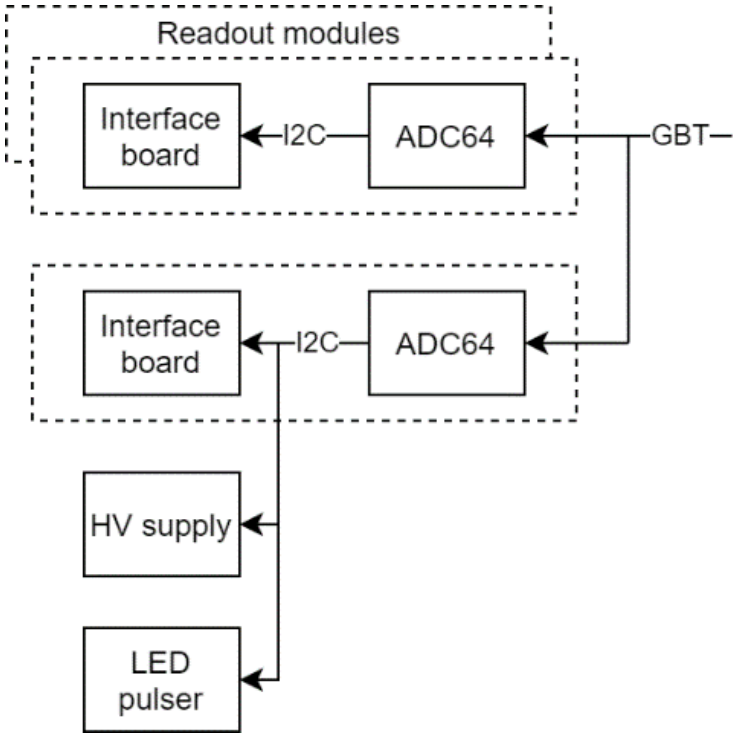


Figure 7 - PSD control scheme

Conclusions

PSD's electronics architecture, consisting of a readout chain and service circuits is ready for production after minor changes in the PCB layouts. All signal path components: sensor boards, cable system and a readout module have been developed and tested on the beam of mCBM

experiment. Service circuits, such as HV bias generator and LED pulse generator have been tested in the lab on the pre-production boards and production PCB design is ready.

References

[1] Serneguet Sorli, ´A. (2015). A multichannel digitizer for the PANDA experiment.
http://hdl.handle.net/10251/56722

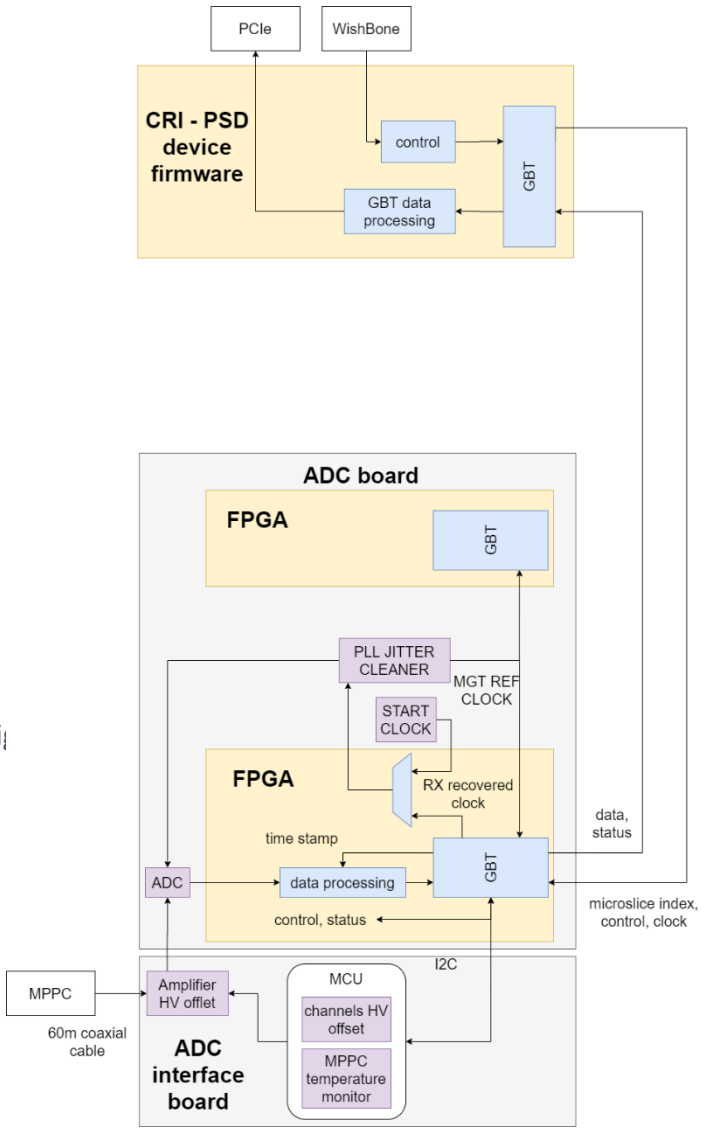
2.2 Full PSD readout chain tests at mCBM (D.Finogeev)

The crucial part of readout development is integration into the experiment common readout system. Each revision of the PSD readout FEE was tested with mCBM DAQ to verify integration possibility into DAQ of CBM experiment. During beam tests at mCBM in June 2021 full PSD readout chain [1] was integrated in CRI (Common Readout Interface) based readout system. One ADC board assembly connected with 60m coaxial cables to MPPC board as the most crucial part of the readout was installed on mCBM in April 2021. ADC and CRI-PSD units firmware, GBT (GigaBit Transceiver) link, clock synchronization, signal propagation through 60 m cable and noise level was verified and current PSD FEE and readout system was accepted to be operation in CBM experiment.

ADC board – CRI communication

The ADC board initially designed for the ECAL detector of PANDA experiment [2] is used for PSD as MPPC signals waveform digitizer. The 64-channel board is based on two Kintex 7 (xc7k160) FPGAs (field-programmable gate array) and LTM9011 ADCs (analog-to-digital converter) with digitization rate up to 125Msps (currently 80MHz is used) and 14-bit resolution. Digitized waveforms are processed in FPGA, event time and charge data will be sent to CRI via GBT link also used for clock distribution and ADC board control. To achieve PSD event time correlation with the whole CBM experiment, ADC clock should be synchronized to CRI board. Switching from local clock to GBT-RX clock procedure was tested with DPB (Data Processing Board) setup at mCBM in 2019.

Figure 1 shows ADC board communication with CRI board. In ADC board clock from TD-100 generator is used for initialization and is forwarded to LMK0460 PLL jitter cleaner. The output of the LMK0460 is the clock source for the MGT transceiver. After GBT RX locks and stabilizes, the input of LMK0460 switches to GBTRX recovered clock. Second FPGA is also connected to CRI via GBT second link and uses ADC and MGTREF clocks from the first FPGA. Time stamp received from CRI is used for measuring event time synchronously to whole CBM DAQ in triggerless readout concept [3].



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ADC firmware

The main task of ADC firmware is hits finding and forwarding measured data to CRI via GBT link. The prototype of the ADC firmware allows analog signals acquisition individually for each channel with triggering by threshold crossing. In final setup the FIR (see next section) filtering procedure with 11 multipliers by channel will be used for pile-up processing and hits finding. Using of the 11 DSP blocks per channel was used in current firmware design for FPGA resources usage estimation.

Current ADC firmware has an option of ‘and’, ‘or’ or ‘async pulser’ triggering combination. Also online monitoring of baseline level, noise RMS value and measuring the readout rate in the range from 0.5 to 4.5MHz are implemented. The possibility to send raw waveforms simplifies the calibration and debugging of PSD readout. Current ADC firmware design use 56% of slice LUTs, 72% of slice FF and 59% of DSPs FPGA resource. Reducing or moving debug and monitoring options to CRI FPGA will simplify ADC firmware at final setup. No FPGA resource limitation for PSD@ADC firmware is expected.

Next steps in ADC firmware development include the change of the ADC clock frequency from 80 to 120 MHz; readout with two active FPGAs and implementation of the signal processing procedure based on FIR filter.

PSD data rate.

PSD FEE digitizes the signals from MPPC with 14bit ADC at a frequency of 80 MHz (will be increased to 120MHz). Signal processing circuity in FPGA can send only the signal parameters such as charge and time because of the link bandwidth limitation. Sending of the raw signal waveform is possible only for debugging and adjustment.

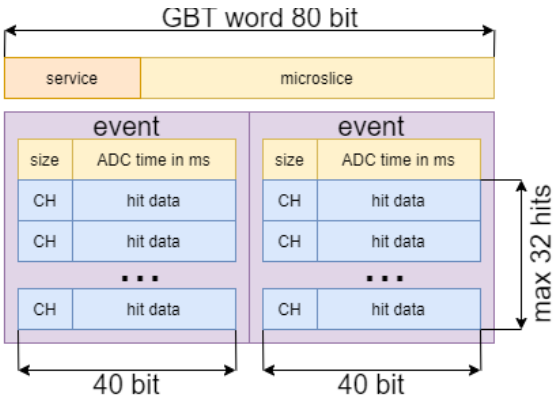

Figure 10 PSD data size concept

Digitized data from the 32 channels per FPGA will be sent via GBT link with 80 bit @ 40 MHz (wide bus GBT mode 120 bit @ 40MHz, without data correction, it is considered as a reserve solution). Time of the single waveform from ADC (hit) is measured related to microslice time in ADC clock cycles. All fired channels in one ADC clock cycle compose event with single header which contain event time in microslice. Preliminarily PSD GBT data format is presented on fig. 1. Single event with hits for 32 channels will consist of 16.5 GBT words or 165 bytes. Maximum event rate for standard GBT mode with 32 hits is 2.4 MHz. Event size from all 16 GBT links is 2.5kB. Expected noise for non-irradiated MPPC at threshold level 0.8 MIP (Minimum Ionization Particle) plus cosmic rate is expected at level 10 Hz per module. That result 460Hz or 74kB/s idle data rate.

CRI-PSD firmware unit

Specific firmware unit was designed for PSD data processing in CBM common readout interface (CRI). The design allow to control FEE system and forward received data from ADC board to FLES (First Level Event Selector) interface. Data taking is also possible through slow control wishbone bus for calibration and debugging purposes. Control and readout software was implemented with python3 macros for beam test in June 2021.

For PSD readout 8 ADC boards in total will be used with 2 GBT link per each board. It is possible to forward 16 GBT links to 8 FLIM interfaces in 2 SLRs. Such topology will exclude start/stop procedure and data buffering in PSD-CRI specific unit. No data throttling is needed in CRI as maximum throughput of FLIM (100 Gb/s) is higher than all 16 GBT link can transmit in wide mode (76,8 Gb/s).

ADC baseline drift

During high intensity tests at mCBM in June 2021, it was found that ADC baseline drifts appeared due to capacitive coupling at the FEE input (Fig. 2). Magnitude of baseline drift is in the order of 15 MIPs that distort energy measurements. Firmware exponential filter compensator was added as a temporary solution for beam tests at mCBM 2021. Compensation filter accuracy ~5% allow to reach good agreement of measured energy spectra with simulation, but accuracy is too low for correct triggering of 1 MIP signals at high rates. Signal is continuously under threshold of 0.8 MIP (1,4mV) level during baseline drift. Developing of the new method of channel self-triggering, based on FIR filter signal processing is ongoing.

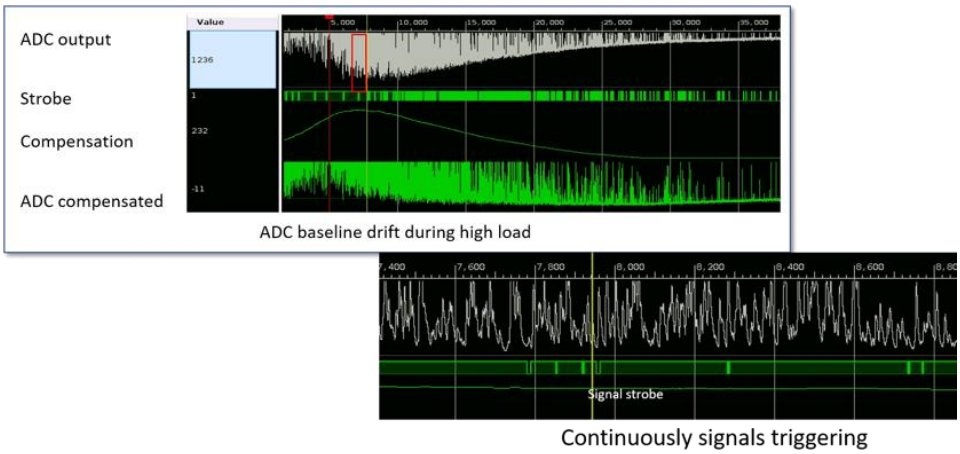

Figure 11 Channel base drift and compensation measured with fpga chipscope

Conclusions

ADC board with ADC board addon, were tested at mCBM beam tests in 2019-2020 with single PSD module (mPSD). Integration into mCBM DAQ based on GBT link was done and time synchronization into the whole detectors system for mPSD hits acquisition was proved.

In 2021 full PSD readout chain prototype which includes ADC board, ADC board addon, MPPC board, 60m coaxial cable for analog signals was assembled at mCBM. Currently the full chain of PSD readout as well as firmware for ADC board and CRI – PSD was successfully tested at mCBM beam high-rate tests in May – June 2021. Good event time correlation between mPSD and mTOF and good correspondence between measured energy spectra and simulated ones was demonstrated. It was demonstrated that the current PSD readout design will be operational at the CBM experiment condition.

References

[1] "The readout system of the CBM Projectile Spectator Detector at FAIR"
DOI: 10.1088/1748-0221/15/09/C09015

[2] Serneguet Sorli, ´A. (2015). A multichannel digitizer for the PANDA experiment.
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2.3 Results of mPSD readout chain tests at mCBM (Karpushkin)

Tests of a full readout chain of the PSD hadron calorimeter were carried out on the test beams of the mCBM experiment. One of the PSD modules (mPSD) with full PSD readout chain was used in these tests. This section describes the algorithms of the signals processing and obtained results.

mPSD at mCBM experiment

The test of a full read-out chain of the mPSD was carried out within the framework of the mCBM experiment [4], a precursor experiment and demonstrator of CBM at FAIR. The mCBM experiment has been set up at the present GSI SIS18 facility, consisting of the detector prototypes or pre-series modules of all CBM detector subsystems including the ultra-fast, triggerless-streaming read-out chains. In this regard, a real-size PSD module has been mounted - the mPSD - for a detailed study of the response of electronics in the conditions close to real. The position of the mPSD in the mCBM experiment is shown schematically in Fig.2.

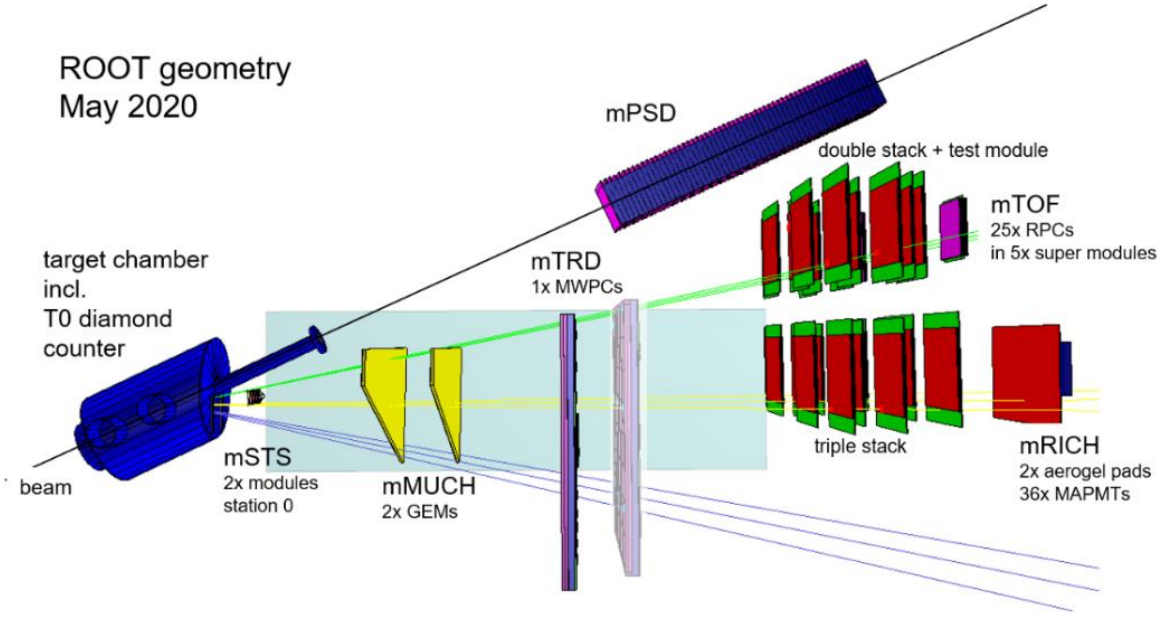

Figure 2. Scheme of the mCBM@SIS18 experiment.

Prony-based signal processing.

The method based on the Prony least squares [1] was used as the offline processing method the digitised signals. This method allows to describe measured discrete amplitudes by a sum of two exponents as shown in the Fig.1, left. Such a parameterization is based on the shape of the scintillator signal and the presence of RC circuits in electronics.

This method of digital signal processing allows to separate the true signals by evaluating the fit quality assessment. The quality of the match between the fitting function and the original signal is assessed by the coefficient of determination (R2) [2]. The Fig.1 on the right shows the dependence

of the R2 on the charge of the fit function of the signal. True muon signals are grouped around zero, while noise and highlighted in a circle pickup signals are grouped near one. The described method is not demanding on computational resources and makes it possible to work with small signals near the noise level and to identify events with overlapping signals.

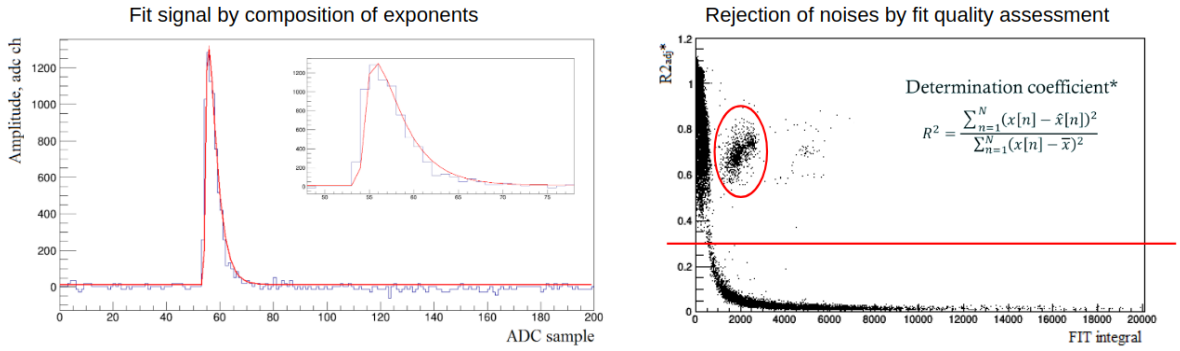

Figure 1. Left: Blue line shows an example of a PSD waveform; the red line is a fitting function calculated by the Prony least squares method. The same waveform on an enlarged scale is shown in the inset on the right. Right: the dependence of the coefficient of determination on the signal charge. True events are located near zero of the coefficient of determination, a group of events with a small charge value and a large coefficient corresponds to noise, red circle indicates a group of events with a pick-up noise.

mPSD calibration with cosmic muons

Before testing the mPSD at beams in mCBM experiment, all sections of the module were calibrated with cosmic muons.

Signal processing was carried out according to the above-described Prony least squares method. The selection of signals from cosmic muons was chosen according to the energy depositions in the sections surrounding the investigated one. The distribution of the energy deposition in the section with various selections is shown in Figure 3.

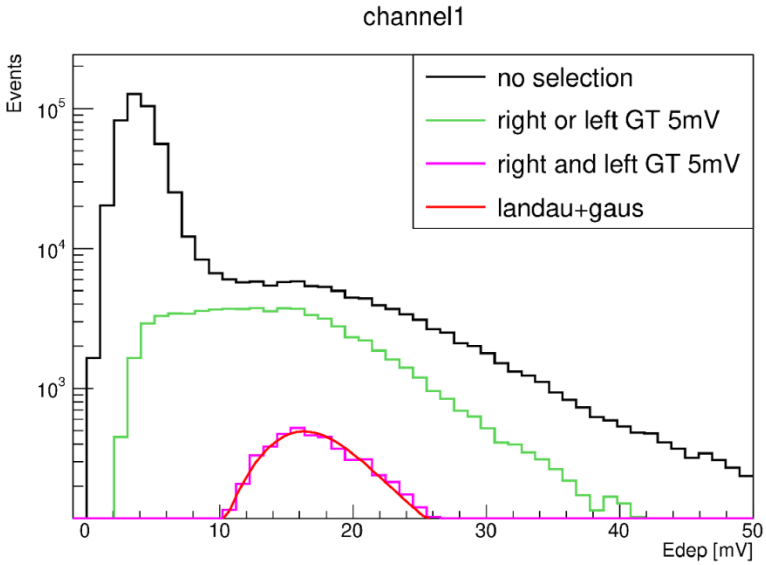

Figure 3 Calibration of mPSD section with cosmic muons

Study of the mPSD response at mCBM

The mCBM beam campaign in summer 2021 used an oxygen ion beam with a kinetic energy of 2 AGeV and a nickel target 4 mm thick. As a result of the tests carried out, it was shown that the data coming from the mPSD is synchronous with the data coming from other mCBM subsystems. The Fig.4 shows the time difference between the mTOF and mPSD data. Clear peak in the distribution marks the obtained time synchronization. The response of the mPSD sections was studied with the beam at various interaction rates and was compared to the simulated data. The maximum interaction rate specified in the PSD TDR, at which calorimeter will be operated, is 1 MHz. During the beam tests at this interaction rate, overlapping signals (pile-ups) accounted for about 35% of the total number of events. In the framework of the analysis, such events with pile-ups were not taken into account.

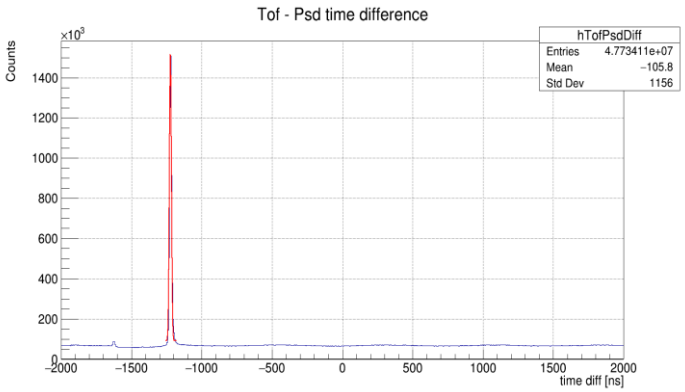

Figure 4. Time difference between mTOF and mPSD data.

Figure 5 shows the comparison of the obtained experimental data in blue and simulated GEANT4 data with FTFP_BERT physics list in magenta. An example of the distribution of energy deposition in the mPSD section #0 is given on the left. The comparison of the energy deposition profiles in the entire mPSD is shown on the right. Here, in each of the ten bins corresponding to the numbers of the mPSD section, the energy deposition averaged over all events is set. In general, the experimental results for the selected events without pile-ups agree well with the simulated data.

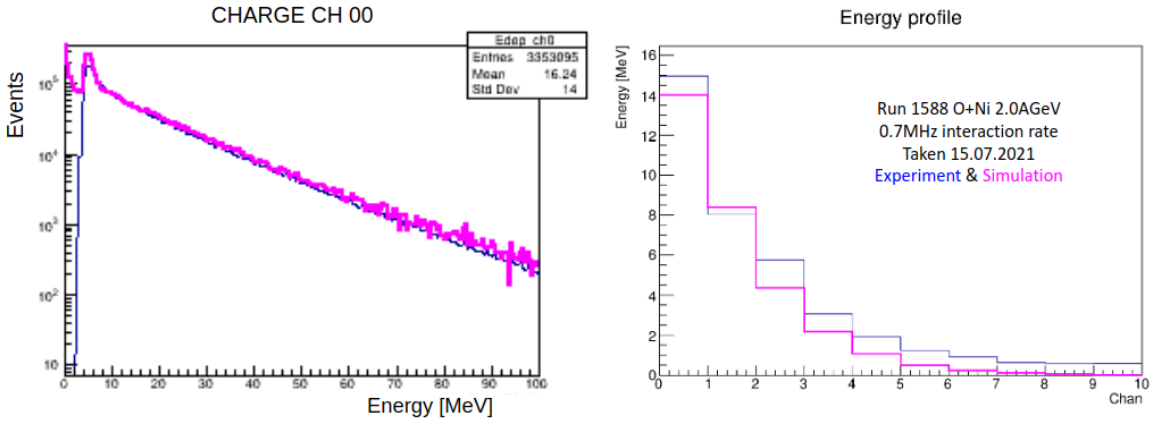

Figure 5. Left: Energy deposition in mPSD section #0 in run 1588 of the mCBM beam campaign compared to simulated data. Right: Energy profile in mPSD compared to simulated data. The data are shown for reaction O+Ni at 2.0AGeV kinetic energy with 4mm Ni target 4mm and interaction rate 0.7MHz.

Issues of the mPSD in beam campaign 2021.

Also, some issues have been identified. First of all, the bandwidth of the GBT link (~100bit/hit) does not allow transmitting signals entirely (~500bit/hit). Thus, it is necessary to implement the signal processing algorithm at the FPGA level. Secondly, baseline drift at high detector loads was observed. Although this effect has been compensated for, this drift makes it no longer possible to effectively trigger on weak signals with an amplitude of about one MIP. And finally, at an interaction rate of about 1 MHz, we observed a large fraction of pile-ups, reaching up to 35%. Therefore, the proposed solution to these issues is the development of a finite impulse response (FIR) digital filter.

FIR filter design.

To create a band-pass filter, the range from 2 to 25 MHz was experimentally selected. With this choice of bandwidth, it is possible to significantly narrow the signals, while not introducing artificial ejections. Cutting the frequency spectrum below 2 MHz eliminates low-frequency fluctuations including the baseline drift, and cutting the spectrum above 25 MHz cuts out high-frequency noise components. Upper picture at the figure 6 shows the waveform of the mPSD signal collected on the beam data with the ADC sampling rate of 80 MHz. Bottom left picture shows the frequency spectrum of the signal and the selected frequency band is highlighted with a dashed line. The frequency response of the designed filter is shown at the bottom right. The designed filter has only 11 coefficients, which makes it possible to implement it in the FPGA.

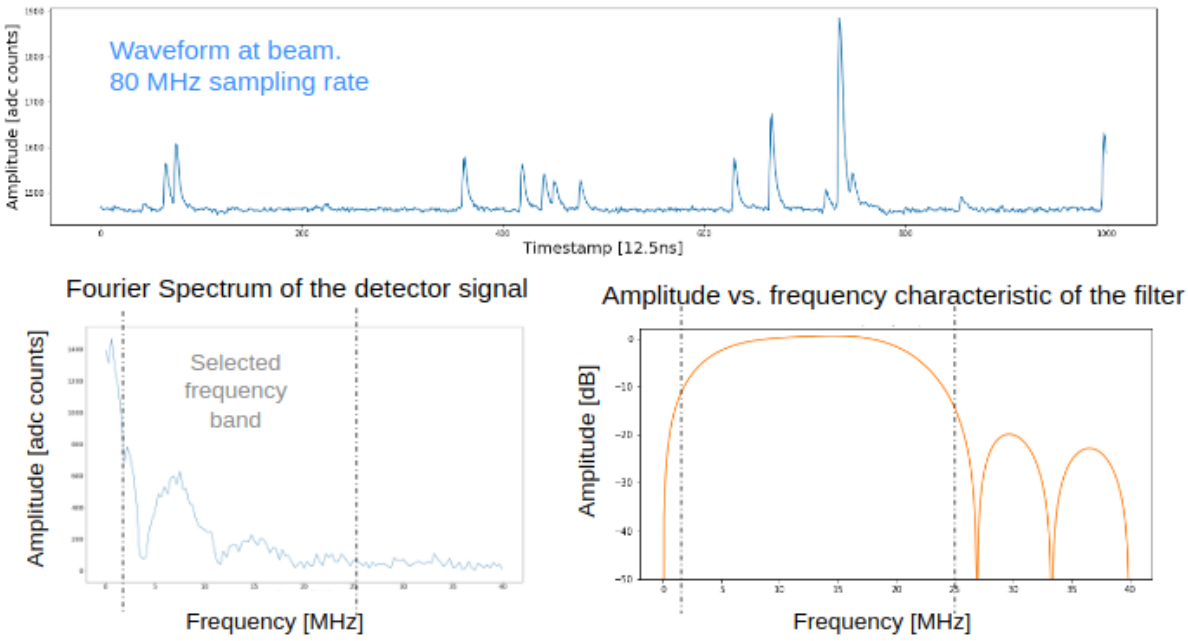

Figure 6. Up: waveform from one mPSD channel taken at beam. Down left: Fourier Spectrum of the detector signal and the selected frequency band. Down right: Amplitude vs. frequency characteristic of the designed filter.

FIR filter application: low-amplitude signals.

The designed filter has been tested for sensitivity to low amplitude signals. Upper part of figure 7 shows signals from cosmic muons (blue). Here, triggering is done by two consecutive points of the waveform exceeding the amplitude threshold (red). Applying the designed filter to the original signals and composing a trigger by the amplitude of

the filtered signal and the sign of its derivative, we got the lower part of figure 6. The analysis shows that the sensitivity to low-amplitude signals near MIP level is completely preserved.

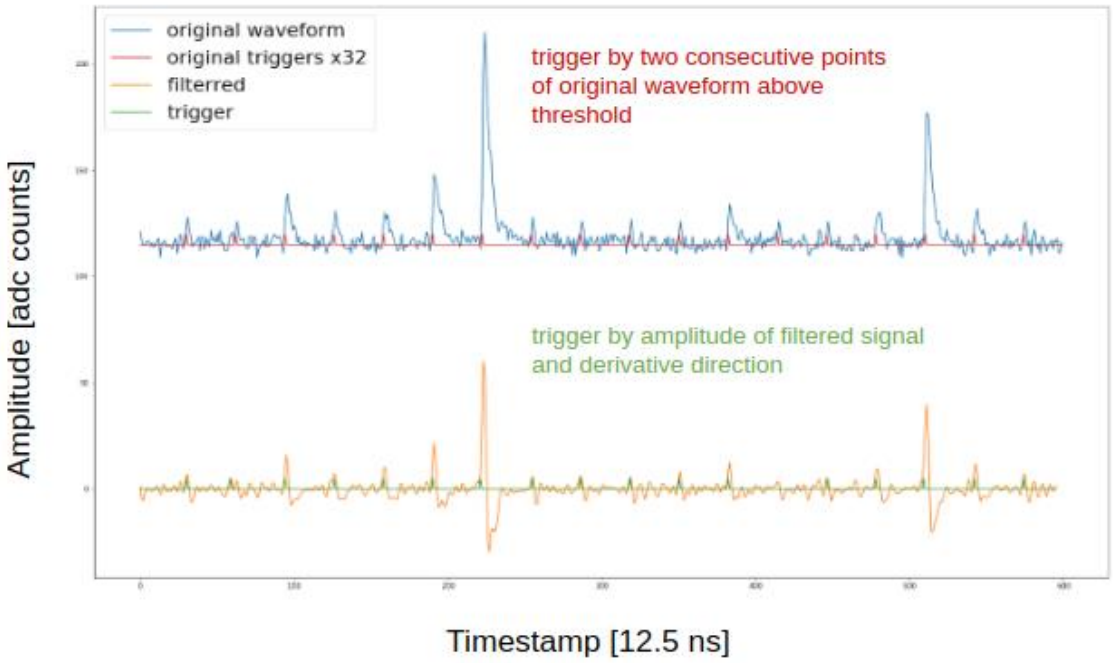

Figure 7. Upper: Cosmic muons signals and previous trigger by two consecutive points exceeding threshold; Lower: filtered signals and new trigger by value of filtered signal and sign of it's derivative.

FIR filter application: pile-ups.

An important point remaining is to determine how well the designed filter can distinguish between pile-ups. For this, 10 examples of the reference signal with different sampling phases were taken and the limiting case was investigated: how close they can be separated from each other, so that the filtered signals have the same amplitudes. The resulting limiting case turned out to be 5 ADC samples, which corresponds to 60 ns. This value was obtained because the filter is designed to be as sensitive as possible to the leading edge of the PSD signals, which is about 5 samples from baseline to maximum. The illustration is given in the Fig.8.

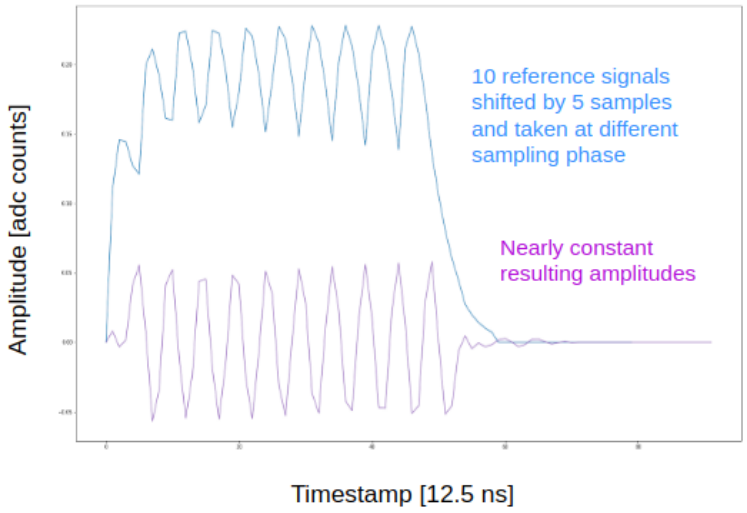

Figure 8. Ten examples of the reference signal with different sampling phases(upper); Nearly constant amplitudes of the filtered signals (lower).

FIR filter: Conclusions.

Thus, the designed digital filter makes it possible to significantly narrow the signal and thus reduce the fraction of events with overlapping signals. Application of the designed filter reduces the fraction of events with pile-ups from 40% of all events to 10% of all events. In addition, it filters out low frequency fluctuations such as a baseline drift and rejects high frequency noise.

Conclusions.

The presented results of testing the complete mPSD readout chain on the mCBM test beams with intensities close to the intensities of the future CBM showed:

1) The designed FEE and readout electronics s fully meets the PSD requirements.
2) mPSD full readout chain tests demonstrate the time synchronization of the mPSD data and the data of other mCBM subsystems.
3) Obtained energy distributions in mPSD longitudinal sections are in good agreement with the simulated data.
4) Application of FIR to the experimental data reduces the fraction of events with pile-ups from 40% of all events to 10% of all events.

References.

1. N.Karpushkin, F.Guber and A.Ivashkin, “Application of the Prony least squares method for fitting signal waveforms measured by sampling ADC” AIP Conference Proceedings 2163, 030006 (2019); https://doi.org/10.1063/1.5130092

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4. CBM Collaboration, “mCBM@SIS18”, doi:10.15120/GSI-2019-00977