Q&A protocol

PSD Electronics and SiPM PRR
https://indico.gsi.de/event/13500/

01.12.2021

List of Questions (Q) and Recommendations (R)

Presentation 1 - Introduction to the PRR of the PSD MPPCs and readout electronics

Q/R from this part are included below, in the specific sections.

Presentation 2 – PRR of PSD MPPCs

Q1: What is the interaction rate you want to operate the PSD (and SiPM) at?

Q2: S/N ratio can be compensated with an over-voltage. How does the latter influence the noise level?

Q3: NIEL effects are discussed. However, there is also total ionizing dose. Can you assess the ionizing radiation effects on SiPM performance? What is the expected ionizing radiation level in the CBM cave? Can ionizing dose make the device (SiPM) also unusable? Is the dose received in the parking position relevant (e.g. from back shine of rear cave wall and beam dump).

It is recommended to check available literature if no tests can be performed.

Q4: Were the devices biased during reported irradiation with neutrons, or not? Can this have any effect on the conclusions?

R5: Please provide consistent irradiation dose values (non-ionizing and ionizing, if available) expected at CBM in one year of operation (define). Clarify necessary SiPM specification and irradiation values obtained in the tests.

Q6: What is the designed calorimeter resolution? Provide comparison to the TDR values. How the resolution for irradiated and non-irradiated SiPMs relate to the designed value?

Q7: What is required dynamic range (lowest/higher energies expected)?

Q8: You show there is no degradation of energy resolution. Do you need to increase the HV for this? Has this any influence on the dynamic range? Is the dynamic range influenced by the irradiation?

Presentation 3 – PRR of FEE and readout electronics (I): Status of PSD electronics development and tests

Q9: Define directives you need to follow. What is the highest voltage you apply in your circuit? What happens in case of a fault? Risk assessment (consider ISO12100 standard) shall be provided (draft now, full risk assessment for the PSD system expected at the time of the FAT).

Q10: You stated that no backplanes are needed for the Wiener plates. How do you power these boards?

Q11: you measure 2 mV signals with no amplifier and use very long cables. Can't you create a ground loop with HV and signal cables?

Q12: Please provide a scheme of the connection, incl. filters, reference potentials, etc. Clarify ground (+safety ground) connection.

Q13: Do you perform irradiation tests with other components, e.g., LEDs?

Q14: How do you produce the PCB and assemble them (not a large number)? Is this outsourced to an external company?

Q15: Clarify production/purchasing timeline of all components, with clear statements on:

- Necessary start of production.
- Production rate and time estimate (incl. global crisis of silicon and PCB industry)
- Complete QA plan and its timeline, incl. QA rate capabilities at the institute
- (Available contingency prior to installation with PSD modules)
- Plan for installation and QA in CBM@FAIR → envisaged steps and necessary time for execution

Q/R16: Controls. Will they be implemented in EPICS, following standard CBM schemes? Control via DAQ channel needs to be re-considered. Can this be avoided? Does it influence the design of the boards?

Presentation 4 – PRR of FEE and readout electronics (II): The full PSD readout chain ntegration and test at the mCBM

Q17: What is your recovery scheme for the SEUs? Do you lose time for synchronization?

R18: Re-initialization scheme shown here can be discussed in the context of TFC development.

Q19: Transmission of 2 mV signals over 60m cables: did you consider differential signals or amplification stage at the module/SiPM level?

Q20: Do you foresee mCBM tests with irradiated SiPMs?

Presentation 5 – PRR of FEE and readout electronics (III): Test results of mPSD with full readout chain at mCBM

Q21: Slide 5 - is the pile-up a rate problem or is it rather a multiple pile up due to multiple hits in one interaction? Are these three independent events shown in the plot?

Q22: You state the rate can be underestimated (which would give additional safety factor for pile-up dependency on rate). Can it be the rate is over-estimated, if it could not be measured properly?

Q23: Analysis was done offline. Eventually, you plan to perform them online on the FPGA. What is your estimation of resources you need for this? Is there enough space in the FPGAs, do you have estimation for all other digital logic which is needed? What is utilization of FPGA?

Q/R24: You have to be sure all your foreseen logic fits into FPGA and there is sufficient space for the future improvements. What is the current reserve?

R25: You limit yourself to 11 DSP blocks. You can consider distributed arithmetic instead of DSP slices. You may need DSP slices for other operations.

Q26: Do you foresee further studies of the filters and FPGA firmware optimization (FPGA resource consumption) with mCBM '22 beam? Provide in the production schedule the time when the decision on FPGA choice needs to be done.

General remarks:

R27: Related to Q23, Q24 and R25: Detection efficiency in a tracking detector (where tracking allows for missing hits) and in a calorimeter (where the whole response is summed) have different impact. In addition, the PSD has a high occupancy for medium-*b* collisions. So hit losses due to pile-up rejects will be highly correlated, and might have significant impact in *b* and event plane reconstruction. It needs to be emphasized, that a CBM pile-up rejection strategy shall be developed, in which the PSD and hit processing in PSD will be critical (together with other systems, e.g. TOF, BFTC, …).

The following questions shall be addressed and the PSD team is asked to provide their assessment and strategy to assess them:
- how will PSD data be analyzed?
- are time ranges with pile-up candidates rejected anyway based on BFTC or TOF?
- how important is good double hit detection in PSD?
- are losses due to pile-up rejection in PSD important?
- if yes, is rejection the right strategy at all?
- do we have a consistent picture here?
- do we have a good overall quality of data assessment here?

Obviously, a CBM-wide discussion is required, which should be triggered with the questions stated above.

Q28: Define number of spare parts and provide rough estimate for a failure rate.

- What is the lifetime of a SiPM and how it relates to the numbers requested in **R5** (CBM year, total radiation dose)?
- How do you define a number of “some” spare parts in your production plans. Do you want to prepare complete front-end PCBs for replacement?
- Did you calulate the lifetime of on year of irradiation? You may want to consider a lto of spares in case of SiPMs.
- Please comment on running/replacement scenarios

Review protocol received by email:

Q29: What is the selection of silicon photo-multipliers studied for using in the project based on?

Answer: The main sample is Hamamatsu MPPC. They are chosen by the key parameters: large number of pixels and short pixel recovery time. The Zekotec MAPDs are the devices already used on hadron calorimeter at NA61/SHINE experiment at CERN. They are used as a reference. The Ketek SiPMs as devices planned to be used at CMS experiment and several samples were in hands to test. The low voltage Sensl are promising devices as well and has been chosen for the radiation tests for the future.

R30: The table of silicon photo-multiplier parameters need to be included in the text pointing the main parameters which need to be studied for irradiation: number of pixels and pulse length.

Answer: Done.

R31: The pulse shape (and recovery time) affects the frequency properties as well.

Answer: This is one of the properties we have chosen. We need to reject effectively expected pile-up signals and therefore the frequency characteristics are very important.

R32: Actually, the signal to noise ratio is an equivalent to the ratio of signal charge to the dark current charge during signal pulse length.

Answer: Based on pp2-4 and the papers studied the properties of silicon photo-multipliers the Hamamatsu MPPC is the best choice.

Q33: Why do you show the current dependency on the radiation dose but not a primary value of frequency of noise pulses? The current depends on the amplification factor and frequency of pulses.

Answer: Unfortunately, the measurement of pure frequency of noise pulses and its dependence of dose is missed. However, the precise device to measure the currents was available at the laboratory so we have a measurement of dark currents. The importance of current measurements is also defined by choosing the design of base voltage source for photo-multipliers. We need to measure the maximum expected current for one channel. The measured values are included in the schematics.

Q34: During the radiation the change of dark current is individual for all MPPCs. Do you expect corrections based on some test measurements on site on the detector on the beam?

Answer: Yes, we will do periodically measurements of light yield change of all MPPCs channels using calibrated light flashes from LED test system. Then the base voltage can be corrected.

Q35: Is the light signal available for each MPPC?

Answer: Yes, we have a single optical fiber for each MPPC. The group of 10 fibers in one PSD module is illuminated with one LED.

Q36: Is 3.3V enough for LED test generator?

Answer: It is a mistake in the text. The value should be 5V. Corrected.

Q37: Light shield of MPPSc:

Answer: Performance of these structures has been tested and showed major reduction of the dark current, from 1 uA (without light shielding) to 80 nA (with light shielding) per MPPC under the same ambient light conditions.

Please clarify: Could it be that what is meant here is not "dark current" but something like "ambient light background"? The dark current should, by definition, not be generated by any light hitting the cathode, so it cannot depend on the light shielding.

Q38: What is a difference of conditions for 1uA and 80nA?

Answer: This is connected to applying the light shielding for MPPSc. Corrected in text.

R39: There is a mistake in the text on slides (see Fig. 5): "*…20 times **less** then expected dose at the PSD.*"

Answer: Yes, should be "more" for sure. Corrected.

Q40: The typical signal length from MPPC is about 10-15ns but you have 80 MS/s digitization rate. Is it enough?

Answer: The length of the signal on the ADC input is defined by signal chain properties. The measured pulse length is about 120-150ns on the ADC. Digitization rate of 80MS/s gives 8-9 points for one pulse.

Q41: Fig.7 – please correct axis (not recognizable).

Answer: Corrected.

Q42: You are using the already developed system for signal digitization based on PANDA ADC board. How well the system is applicable for PSD signal shapes?

Answer: In 2019 the tests were done for preliminary signal digitization capability for MPPC with PANDA ADC board. As a result the addon board has been designed and constructed. The signals from MPPC have an amplification and base line shift for using full scale range of input stage of ADC board (2Vpp).

Q43: Please comment the procedures of time and charge characterizations of pulse shape. What are the possible errors and algorithms of their compensations?

Answer:

The sections 2.2 has a description of clock time synchronization and time of event measurement:

The ADC is synchronized with all detector systems. Each clock the ADC board has a timestamp which is connected to all detectors as well. The hit time is measured with respect to the timestamp of threshold crossing. The charge is calculated for the fix window length (32 points of ADC). The signal position can be tuned in a program. Currently the new algorithm based on the FPGA FIR filter is under development for charge and time measurements. The analysis of reference signals shows the maximum error of charge determination on the level of 15%.